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EXAMINER	
FENNEMA, ROBERT E	
ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,331	TAN ET AL.	
	Examiner	**Art Unit**	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 have been considered.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5-10, 12-14, 16-21, 23-24, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Tredennick et al. (USPN 4,338,661, herein Tredennick).

4. As per Claim 1, Tredennick teaches: A microprocessor, comprising:

a microcode ROM (Column 15, Lines 33-34), wherein a row in the microcode ROM stores a plurality of groups of microcode operations (Column 15, Lines 36-37), wherein a group of the plurality of groups of microcode operations is comprised in a microcode routine (Column 1, Lines 55-56), and wherein the row stores an associated control sequence for each of the plurality of groups of microcode operations (Column 15, Lines 52-55 and Lines 59-66); and

a control sequence logic unit coupled to the microcode ROM (Figure 4, Address Selection 64), wherein in response to accessing the group of microcode operations comprised in the microcode routine, the control, sequence logic unit is configured to use the control sequence associated with the group of microcode operations to identify an

other row storing one or more next groups of microcode operations comprised in the microcode routine(Column 15, Lines 37-40, it selects the next line of the ROM, which is output from the microcode ROMs as shown in Column 15 Lines 52-55 and 59-66).

5. As per Claim 2, Tredennick teaches: The microprocessor of claim 1, wherein at least one of the plurality of groups of microcode operations stored in the row is part of a different microcode routine (Figure 11, also see Column 19, Lines 52-55).

6. As per Claim 3, Tredennick teaches: The microprocessor of claim wherein the control sequence logic unit is configured to identify which of a plurality of groups of microcode operations stored in the other row of the microcode ROM are comprised in the microcode routine based on information contained in the control sequence associated with the group of microcode operations stored in the row (Column 15, Lines 52-55 and 59-66, which defines which row and position the next group is located).

7. As per Claim 5, Tredennick teaches: The microprocessor of claim 1, wherein if the group of microcode operations comprises at least one branch operation, the control sequence logic unit is configured to identify the next group of microcode operations in the microcode routine dependent on a branch prediction as well as the control sequence associated with the group of microcode operations (Column 15, Lines 49-55 teach a microcode instruction for branches, and Column 17 Lines 29-32 show that the outcome either way will be in the same row specified by the control sequence).

8. As per Claim 6, Tredennick teaches: The microprocessor of claim 1, wherein the microcode ROM is divided into a plurality of segments, wherein a same number of groups of microcode operations is stored in each row of a given one of the plurality of segments, and wherein each row in the given one of the plurality of segments stores a different number of groups of microcode operations than each row in each other one of the plurality of segments (Column 19, Lines 22-27. It is disclosed that for each row, the address may represent one, two, four, or up to eight different groups. So there are segments in the sense that some lines can contain a different number of groups than the other lines).

9. As per Claim 7, Tredennick teaches: The microprocessor of claim 6, wherein groups of microcode operations stored in a same one of the plurality of segments have a same maximum width (Column 19, Lines 22-27).

10. As per Claim 8, Tredennick teaches: The microprocessor of claim 7, wherein groups of microcode operations stored in one of the plurality of segments have a maximum width that is different from a maximum width of groups of microcode operations stored in another one of the plurality of segments (Column 19, Lines 22-27).

11. As per Claim 9, Tredennick teaches: The microprocessor of claim 8, wherein one of the plurality of segments stores one group of microcode operations and one associated control sequence per row (Column 19, Lines 22-27).

12. As per Claim 10, Tredennick teaches: The microprocessor of claim 6, wherein the control sequence logic unit is configured to identify a position of one or more groups of microcode operations and a position of one or more control sequences dependent on which of the plurality of segments of the microcode ROM stores the one or more groups of microcode operations (Column 15, Lines 52-55 and 59-66, which defines which row and position the next group is located).

13. As per Claim 12, Tredennick teaches: A computer system, comprising:

a system memory (Column 4, Lines 54-56); and

a microprocessor coupled to the system memory (Column 4, Lines 51-52), comprising;

a microcode ROM (Column 15, Lines 33-34), wherein a row in the microcode ROM stores a plurality of groups of microcode operations (Column 15, Lines 36-37), wherein one of the plurality of groups of microcode operations is comprised in a particular microcode routine (Column 1, Lines 55-56), and wherein the row stores an associated control sequence for each of the plurality of groups of microcode operations (Column 15, Lines 52-55 and Lines 59-66); and

a control sequence logic unit coupled to the microcode ROM (Figure 4, Address Selection 64), wherein in response to accessing the group of microcode operations comprised in the microcode routine, the control sequence logic unit is configured to use the control sequence associated with the group of microcode operations to identify an other row storing one or more next groups of microcode operations comprised in the microcode routine (Column 15, Lines 37-40, it selects the next line of the ROM, which is output from the microcode ROMs as shown in Column 15 Lines 52-55 and 59-66).

14. As per Claim 13, Tredennick teaches: The computer system of claim 12, wherein at least one of the plurality of groups of microcode operations stored in the row is part of a different microcode routine (Figure 11, also see Column 19, Lines 52-55).

15. As per Claim 14, Tredennick teaches: The computer system of claim 12, wherein the control sequence logic unit is configured to identify which of a plurality of groups of microcode operations stored in the other row of the microcode ROM are comprised in the microcode routine, based on information contained in the control sequence associated with the group of microcode operations stored in the row (Column 15, Lines 52-55 and 59-66, which defines which row and position the next group is located).

16. As per Claim 16, Tredennick teaches: The computer system of claim 12, wherein if the group of microcode operations comprises at least one branch operation, the control sequence logic unit is configured to identify the next group of microcode

operations in the microcode routine dependent on branch prediction as well as the control sequence associated with the group of microcode operations (Column 15, Lines 49-55 teach a microcode instruction for branches, and Column 17 Lines 29-32 show that the outcome either way will be in the same row specified by the control sequence).

17. As per Claim 17, Tredennick teaches: The computer system of claim 12, wherein the microcode ROM is divided into a plurality of segments, wherein a same number of groups of microcode operations is stored in each row of any of the plurality of microcode ROM segments, and wherein the number of groups of microcode operations stored in a row in one of the plurality of microcode ROM segments differs from the number of groups of microcode operations stored in a row in another one of the plurality of microcode ROM segments (Column 19, Lines 22-27. It is disclosed that for each row, the address may represent one, two, four, or up to eight different groups. So there are segments in the sense that some lines can contain a different number of groups than the other lines).

18. As per Claim 18, Tredennick teaches: The computer system of claim 17, wherein groups of microcode operations stored in any one of the plurality of microcode ROM segments have a same maximum width (Column 19, Lines 22-27).

19. As per Claim 19, Tredennick teaches: The computer system of claim 18, wherein groups of microcode operations stored in one of the plurality of microcode ROM

segments have a maximum width that is different from a maximum width of groups of microcode operations stored in another one of the plurality of microcode ROM segments (Column 19, Lines 22-27).

20. As per Claim 20, Tredennick teaches: The computer system of claim 19, wherein one of the plurality of microcode ROM segments stores one group of microcode operations and one associated control sequence per row (Column 19, Lines 22-27).

21. As per Claim 21, Tredennick teaches: The computer system of claim 17, wherein the control sequence logic unit is configured to identify a position of one or more groups of microcode operations within a row and their associated control sequences dependent on which of the plurality of segments of the microcode ROM stores the one or more groups of microcode operations (Column 15, Lines 52-55 and 59-66, which defines which row and position the next group is located).

22. As per Claim 23, Tredennick teaches: A method, comprising:

storing a plurality of groups of microcode operations (Column 15, Lines 36-37) and a plurality of control sequences in a row in a microcode ROM, wherein each of the plurality of control sequences is associated with a respective one of the groups of microcode operations (Column 15, Lines 52-55 and Lines 59-66); and

in response to accessing one of the plurality of groups of microcode operations, using the one of the plurality of control sequences associated with that one of the

plurality of groups to identify a next group of microcode operations to output from the microcode ROM (Column 15, Lines 37-40, it selects the next line of the ROM, which is output from the microcode ROMs as shown in Column 15 Lines 52-55 and 59-66).

23. As per Claim 24, Tredennick teaches: The method of claim 23, further comprising identifying the next group of microcode operations based on one or more branch predictions as well as the one of the plurality of control sequences if the one of the plurality of groups of microcode operations includes one or more branch operation (Column 15, Lines 49-55 teach a microcode instruction for branches, and Column 17 Lines 29-32 show that the outcome either way will be in the same row specified by the control sequence).

24. As per Claim 27, Tredennick teaches: A system, comprising:

a microcode ROM (Column 15, Lines 33-34), wherein a row in the microcode ROM stores a plurality of groups of microcode operations (Column 15, Lines 36-37) and wherein the row stores an associated control sequence for each of the plurality of groups (Column 15, Lines 52-55 and Lines 59-66); and

means for accessing a control sequence associated with one of the plurality of groups of microcode operations and responsively accessing a next group of microcode operations stored in the microcode ROM (Column 15, Lines 37-40, it selects the next line of the ROM, which is output from the microcode ROMs as shown in Column 15 Lines 52-55 and 59-66).

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 4, 11, 15, 22, and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tredennick, in view of Yoshida (USPN 5,761,470).

27. As per Claim 4, Tredennick teaches the microprocessor of claim 3, but fails to teach: wherein if fewer than all of a plurality of groups of microcode operations stored in the other row of the microcode ROM are comprised in the microcode routine, the control sequence logic unit is configured to substitute NOPs for the microcode operations comprised in the groups not comprised in the microcode routine when outputting the row to the scheduler.

Yoshida teaches of a VLIW machine, which exploits parallelism by executing multiple instructions simultaneously, where one VLIW word can specify a plurality of instructions (Column 1, Lines 25-30), much as a microcode ROM row specifies a plurality of instructions (groups). This parallelism allows the processor to execute at a high speed, allowing for faster performance (Column 1, Lines 17-20). Yoshida also teaches that the conventional VLIW machine cannot execute an instruction from the word in parallel, it inserts a NOP in its place, as it has to execute some instruction

(Column 1, Lines 51-56). Given the advantage of higher speed through parallelism, one of ordinary skill in the art at the time the invention was made would have converted Tredennick's invention to operate in a parallel fashion such as a VLIW machine to increase the speed and performance.

28. As per Claim 11, Tredennick teaches the microprocessor of claim 1, but fails to teach: wherein a plurality of groups of microcode operations stored in the other row of the microcode ROM are comprised in the microcode routine and are output during a single access.

Yoshida teaches of a VLIW machine, which exploits parallelism by executing multiple instructions simultaneously, where one VLIW word can specify a plurality of instructions (Column 1, Lines 25-30), much as a microcode ROM row specifies a plurality of instructions (groups). This parallelism allows the processor to execute at a high speed, allowing for faster performance (Column 1, Lines 17-20). Given the advantage of higher speed through parallelism, one of ordinary skill in the art at the time the invention was made would have converted Tredennick's invention to operate in a parallel fashion such as a VLIW machine to increase the speed and performance.

29. As per Claim 15, Tredennick teaches the computer system of claim 14, but fails to teach: wherein if fewer than all of a plurality of groups of microcode operations stored in the other row of the microcode ROM are comprised in the microcode routine, the control sequence logic unit is configured to substitute NOPs for the microcode

operations comprised in the groups not comprised in the microcode routine when outputting the row to the scheduler.

Yoshida teaches of a VLIW machine, which exploits parallelism by executing multiple instructions simultaneously, where one VLIW word can specify a plurality of instructions (Column 1, Lines 25-30), much as a microcode ROM row specifies a plurality of instructions (groups). This parallelism allows the processor to execute at a high speed, allowing for faster performance (Column 1, Lines 17-20). Yoshida also teaches that the conventional VLIW machine cannot execute an instruction from the word in parallel, it inserts a NOP in its place, as it has to execute some instruction (Column 1, Lines 51-56). Given the advantage of higher speed through parallelism, one of ordinary skill in the art at the time the invention was made would have converted Tredennick's invention to operate in a parallel fashion such as a VLIW machine to increase the speed and performance.

30. As per Claim 22, Tredennick teaches the computer system of claim 12, but fails to teach: wherein a plurality of groups of microcode operations stored in the other row of the microcode ROM and comprised in the microcode routine are output during a single access.

Yoshida teaches of a VLIW machine, which exploits parallelism by executing multiple instructions simultaneously, where one VLIW word can specify a plurality of instructions (Column 1, Lines 25-30), much as a microcode ROM row specifies a plurality of instructions (groups). This parallelism allows the processor to execute at a

high speed, allowing for faster performance (Column 1, Lines 17-20). Given the advantage of higher speed through parallelism, one of ordinary skill in the art at the time the invention was made would have converted Tredennick's invention to operate in a parallel fashion such as a VLIW machine to increase the speed and performance.

31. As per Claim 25, Tredennick teaches the method of claim 23, but fails to teach: further comprising substituting NOPs for one or more groups of microcode instructions stored in a same row as the next group of microcode operations dependent on the one of the plurality of control sequences.

Yoshida teaches of a VLIW machine, which exploits parallelism by executing multiple instructions simultaneously, where one VLIW word can specify a plurality of instructions (Column 1, Lines 25-30), much as a microcode ROM row specifies a plurality of instructions (groups). This parallelism allows the processor to execute at a high speed, allowing for faster performance (Column 1, Lines 17-20). Yoshida also teaches that the conventional VLIW machine cannot execute an instruction from the word in parallel, it inserts a NOP in its place, as it has to execute some instruction (Column 1, Lines 51-56). Given the advantage of higher speed through parallelism, one of ordinary skill in the art at the time the invention was made would have converted Tredennick's invention to operate in a parallel fashion such as a VLIW machine to increase the speed and performance.

32. As per Claim 26, Tredennick teaches the method of claim 25, but fails to teach: wherein the groups of microcode operations comprised in the microcode routine and the NOPs are output as a single line.

Yoshida teaches of a VLIW machine, which exploits parallelism by executing multiple instructions simultaneously, where one VLIW word can specify a plurality of instructions (Column 1, Lines 25-30), much as a microcode ROM row specifies a plurality of instructions (groups). This parallelism allows the processor to execute at a high speed, allowing for faster performance (Column 1, Lines 17-20). Given the advantage of higher speed through parallelism, one of ordinary skill in the art at the time the invention was made would have converted Tredennick's invention to operate in a parallel fashion such as a VLIW machine to increase the speed and performance.

Response to Arguments

33. Applicant's arguments filed 7/10/2006 have been fully considered but they are not persuasive.

Firstly, regarding Claim 1, Applicant has argued that Tredennick fails to teach anywhere in the citation that a row in the ROM stores a plurality of groups of microcode operations, comprising a microcode routine, with a control sequence associated with each group to identify an other row storing the next groups of instructions. For further clarification of a row in the ROM containing multiple "groups", see Column 19, Lines 23-27, which had been previously referred to in claims such as Claim 6. Column 1, Lines 55-56 show that these instructions are part of a microcode routine, and Column 15,

Lines 52-55 and 59-66 show that each word (group) has a control which specifies the address to the next address, which must identify a row in order to continue to use the ROM. Therefore, Tredennick teaches each and every limitation of Claim 1, in addition to Claims 12 and 23, which include limitations similar to Claim 1, in addition to Claim 27, which has similar limitations, except the control addresses a group instead of a row, which is taught by Tredennick as explained above.

As per Claims 2 and 13, Figure 11 clearly shows that each row contains multiple instructions of different types, thus, different groups. As group has been given no solid definition in the claims, different groups have been interpreted as different instructions. Figure 11 also for this reason shows each line containing multiple groups per row.

As per Claims 3 and 14, Examiner disagrees with Applicant's arguments that an address does not specify a row and position for the next group. The cited portion discloses that the address directs the processor to the next group in the routine, which must specify a row, as discussed in Claim 1. It can be further seen in Figure 11a that the 10 bit address does select a position using bits A1 and A0.

As per Claims 5, 16, and 24, in a similar manner to Claim 3, Tredennick teaches that the branch outcomes must be in the same row of the microcode ROM (further providing evidence of multiple groups per ROM row, which Applicant asserted was not taught in the reference). Applicant has argued that Tredennick teaches away from the claims because both outcomes are located in the same row. However, Tredennick teaches this is done to minimize the size of the storage, to prevent multiple instances of the branch from being put in memory (Column 2, Lines 40-50), and as explained above,

Tredennick can specific positions inside a row, the fact that they are in the same row is a space optimization.

As per Claims 6 and 17, Applicant has argued a "word line" in Tredennick is not a row, but instead, teaches a selects a single microword or nanoword. However, In Tredennick, the world line in one ROM is a row (the micro ROM), or a "group" in the nano ROM. Thus, when reading Tredennick as it was intended, a "row" or "word" in the micro ROM corresponds to <u>multiple</u> "words" in the nano ROM. Tredennick further teaches, in Column 19, Lines 23-27, that the nano ROM may represent one, two, four, or up to eight different groups, and that each line may do so, which the Examiner had interpreted such that each line may have one, two, four, or eight associated groups/operations, such that "segments" were formed, based on the number of groups in each corresponding micro ROM row. By the same reasoning, Tredennick reads on Claims 7-9 and 18-20.

As per Claims 10 and 21, the arguments made are substantially similar to the arguments for Claims 3 and 14, and Examiner refers Applicant to the arguments for those Claims.

Furthermore, Applicant has argued the combination of Yoshida with Tredennick, because it would "clearly and dramatically change the principle of operation of his invention". Examiner disagrees. Tredennick's invention is essentially a machine which executes instructions using microcode stored in a ROM. Modifying the invention to work in a parallel manner does not affect this principle in any way, shape, or form. While the modification to make parallel may change certain elements of the invention, the overall

principle of the invention will remain the same, to execute instructions. Therefore, the inclusion of Yoshida is proper, as the principle of the invention has not changed in any way.

In response to applicant's arguments in Claims 4, 15, and 25, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Yoshida does not need to teach the structural elements of the claim, Tredennick is used for that purpose. Yoshida is used to show that one of ordinary skill in the art would have recognized the need to insert NOP's in place of instructions fed to the machine that could not be executed in order to ensure correct execution, which is a motivation for doing so to one of ordinary skill in the art.

Furthermore, in response to applicant's arguments in Claims 11, 22, and 26, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Yoshida does not need to teach instructions stored in rows in a ROM, and the other structural elements of the claim, that is what Tredennick was used to teach .Yoshida

provides motivation for accessing multiple groups of the groups in the row that Tredennick teaches, to increase performance by being able to potentially execute multiple operations at once, and that one of ordinary skill in the art would have been able to modify Tredennick to do so.

Conclusion

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert E Fennema
Examiner
Art Unit 2183

RF

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SUPERVISORY PATENT EXAMINER
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